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Authors: Seyedehmarzieh Rouhani[1], Kasra Rouhi[2], Adib Abrishamifar[3], Majid Tayarani[4]

Affiliations: Iran University of Science and Technology[1]

Orcid ids: 0000-0002-5362-5624[1], 0000-0002-1226-0104[2]

Contact e-mail: smrouhanie@elec.iust.ac.ir

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Increased Efficiency of a Current Compensating Load Modulation Based MMIC Doherty Power Amplifier Design In 0.25 μm GaAs pHEMT Technology

Seyedehmarzieh Rouhani, Kasra Rouhi, Adib Abrishamifar¹, Majid Tayarani

School of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran, Tel: +98(21) 73225727,
Fax: +98(21) 73225777

Abstract

In this work, a premise is applied to the conventional load modulation equation of Doherty power amplifier (DPA) in 0.25 μm GaAs pHEMT technology to compensate output impedance of main amplifier ($Z_{out,main}$) variation, even in low power region. Using this modified modulation leads to the DPA's power added efficiency (PAE) increase in comparison by the case in which the load modulation revision is ignored, which is also designed in this paper. Second harmonic rejection networks are also added to both designs to play their roles as to efficiency increase. By doing so, the revised load modulation based DPA has the maximum PAE of 39.6%, maximum output power (P_{out}) of 31.61dBm, at 8 GHz. Simulation results of this DPA in higher harmonics indicate the designed DPA has the minimum second and third harmonics power of -51.7 dBm and -80 dBm, respectively. For the sake of linearity evaluation, it is depicted that 1dB-power gain compression has not occurred in the input power (P_{in}) range in which the proposed DPA works.

Key Words: Doherty, High Efficiency, Load Modulation, PAE, Power Amplifier

1. Introduction

The galloping rate of progress in global wireless communication based on which the outermost parts of the world are in contact needs high efficient transceivers by which the demand of portable devices assigned for the mass communication can be met[1-5]. Power amplifiers as subsystems in transceivers always have been in great interest of research [6-25] due to their influence on the efficiency and linearity of whole systems. There is a plethora of novel structures and models proposed to develop PA's efficiency and linearity, such as envelope tracking [26], out-phasing [27], class E and class F PAs [11, 28], DPA [29], to name but a few. Among them, DPA has received dramatic acceptance due to its compatibility to deal with the increased PAPR signals [29]. The main concept of DPA is grounded on its load modulation [29], which is done by a $\lambda/4$ transmission line (TL). Many designers have used the Doherty technique to present high-efficiency performance in different technologies in which their proposed PAs were simulated or manufactured [30-33]. Still, there is a delicate point that should be noticed, and this fact is that $Z_{out,main}$ can vary differently by the level of power it receives in disparate technologies. In other words, $Z_{out,main}$'s impedance trajectory can indicate considerable variation by different power levels delivered to the main amplifier (PA_{main}) even in the low power region. Therefore, in this case, the conventional equation of load modulation needs some more consideration and revision. In this work, using GaAs MMIC technology, the load modulation equation is revised according to the variation of $Z_{out,main}$ trajectory in both low and high power regions. Because imposing our proposed change to load modulation leads to a change in output currents ratio of both PA_{main} and auxiliary power amplifier (PA_{aux}), we call this revised equation as current compensated load modulation

¹ Corresponding author.

E-mail addresses: smrouhanie@elec.iust.ac.ir (S.Rouhani), kasrarouhi@elec.iust.ac.ir (K.Rouhi)
abrishamifar@iust.ac.ir, (A.Abrishamifar), m_tayaran@iust.ac.ir (M.Tayaran)

(CCLM). Applying this compensation for both power levels has resulted in an efficiency increase in comparison by the case in which the impedance change mentioned above was ignored- the conventional load modulation was utilized. This comparison is also provided in this paper and verifies a modified load modulation utilization's advantages.

2. Theory and steps of the DPA design

DPA enjoys two paths of amplification, PA_{main} and PA_{aux} . The first one commences power amplification as it receives power, and it is biased as a class AB PA while the second PA, which operates as a class C PA, is in off state. When the P_{in} increases, the PA_{aux} contributes to amplification, and for the sake of reaching the maximum possible efficiency, load modulation is done by a $\lambda/4$ TL (see Eq.1). Because different technologies don't change alike, and there is no solid guarantee that $Z_{out,main}$ will be constant at the entire low-level power region in all technologies, it seems the equation of load modulation needs some modification. Otherwise, the efficiency in both low and high-level power will not be as well as it is expected. In the conventional load modulation equation, we have:

$$Z_{out,main} = \frac{Z_0^2}{R_L} - Z_0 \frac{i_{aux}}{i_{main}} \quad (1)$$

To modify Eq.1, Z_0 and $\frac{i_{aux}}{i_{main}}$ are replaced by Z_0' and $(i_{aux}/i_{main})'$ respectively. At first, it is assumed that there is a linear equation between them (see Eq.2), then the design will be done under these premises. At this point, if the efficiency becomes considerably better than that of the conventional load modulation based design, these assumptions will be accepted. Otherwise, those premises will be changed, and non-linear equations between the parameters mentioned above will be set. The following relations show the procedure of making some changes in the conventional load modulation equation.

At first, we assume:

$$\begin{cases} Z_0' = nZ_0 \\ (i_{aux}/i_{main})' = \alpha(i_{aux}/i_{main}) \end{cases} \quad (2)$$

According to load-pull simulation results, at high power region $\overline{Z_{out,main}} \approx 1.2 \times \overline{Z_{out,main}'}$ (this point can also be interpreted from Fig.5, $\overline{Z_{out,main}}$ is average of $Z_{out,main}$), by applying this equation to load modulation, we have:

$$\frac{Z_0^2}{R_L} - Z_0 \frac{i_{aux}}{i_{main}} \approx 1.2 \times \left(\frac{Z_0'^2}{R_L} - Z_0' \left(\frac{i_{aux}}{i_{main}} \right)' \right) \quad (3)$$

By putting Eq.2 in Eq.3 and with some simplification, we have the following equation:

$$\frac{(1.2n^2 - 1)Z_0^2}{R_L} - (1.2\alpha n - 1)Z_0 \left(\frac{i_{aux}}{i_{main}} \right) = 0 \quad (4)$$

After some simplification, we have:

$$\frac{(1.2n^2 - 1)Z_0}{(1.2\alpha n - 1)R_L} = \left(\frac{i_{aux}}{i_{main}} \right) \quad (5)$$

From microwave concepts and principle [34], we know:

$$Z(x) = \frac{V(x)}{I(x)} = \frac{V^+(x) + V^-(x)}{I^+(x) - I^-(x)} \quad (6)$$

Here to compensate for the varied $Z_{out,main}$, it is surmised that a modified Z_0 is needed, which is shown by Z_0' . If the variation in voltage and current with power (due to impedance variation) is rewritten with Γ the Eq.6 changes as follows:

$$Z(x) = \frac{V^+(x) + \Gamma V^+(x)}{I^+(x) - \Gamma I^+(x)} \xrightarrow{Z_0 = \frac{V^+(x)}{I^+(x)}} Z(x) = \left(\frac{1 + \Gamma}{1 - \Gamma} \right) Z_0 = Z_0' \xrightarrow{(2)} n = \frac{1 + \Gamma}{1 - \Gamma} \quad (7)$$

In conventional DPA, it was assumed that in the low-power region reflection coefficient is equal by zero ($\Gamma = 0$). Still, in this case, to model the effect of $Z_{out,main}$ change in load modulation, the worst amount of Γ in this power region is chosen by which we can find out the new ratio of PA_{main} and PA_{aux} 's currents, $(i_{aux}/i_{main})'$. According to the load-pull simulation results, the most change of $Z_{out,main}$ in the low-power region leads to $\Gamma = 0.25$. By putting $\Gamma = 0.25$ at Eq.7, we have $n \approx 1.7$. By solving Eq.5 with this amount of n , one can find out $\alpha \approx 1.7$ ($(i_{aux}/i_{main}) = 1$ is assumed).

Now the effect of $Z_{out,main}$ change in both low and high power regions is modeled. The next step is to find PAs' proper size to satisfy the $(i_{aux}/i_{main})'$ ratio discussed in the next section.

Fig1. Schematic of the proposed DPA under CCLM premise (the elements in grey boxes are the last and the first elements of OMN and IMN of first and second stages PAs, which are merged together in circuit's layout, and the exact amount of all elements is provided in Appendix).

Fig2. Schematic of the conventional load modulation based DPA (the elements in the grey boxes are the last and the first elements of OMN and IMN of first and second stages PAs, which are merged together in circuit's layout, and the exact amount of all elements is provided in Appendix).

2.1. Size selection

There are several choices by which the desired $(i_{aux}/i_{main})'$ ratio can be satisfied. The confining factor for picking the proper one is the stability of the circuit [35]. In the technology this work is designed, the bigger transistor has the stabilizer network with less power gain degradation, a parallel RC network whose capacitance is more, can be utilized. According to this point, the biggest size transistor is chosen, which is $8 \times 150 \mu m$ for PA_{main} then the size of auxiliary ones will be set proportionally to satisfy the $(i_{aux}/i_{main})'$ ratio condition. It should be noticed that, according to [36], instability before 1 GHz for $8 \times 150 \mu m$ -transistor

can be ignored. Fig.3 indicates the effect of the transistor's size and its stability by using a stabilizer network.

Fig.3. Stability of the largest and the smallest transistors in 0.25 μ m pHEMT GaAs technology with stabilizer networks for each one.

2.2. Bias consideration

According to the concept of IP3, in multi-stage structures, designers should take more care about the linearity of the last stages [35]. Therefore, in this work, the first stage of PA_{aux} is biased as a deep class C PA while the second one is designed in a soft class C PA. In the main path, both gate stages' biases are set the same because their inherent behavior is linear.

2.3. Phase consideration

In a conventional DPA configuration, a $\lambda/4$ TL is put at the input of auxiliary way to compensate for the added 90° phase in the main path of amplification due to the presence of a $\lambda/4$ TL contributing to the load modulation [29]. This phase compensation can be done in matching networks of PA_{main} , no matter in input or inter-stage or output stage matching networks (IMNs, ISMNs, OMNs). Considering the amount of phase should be compensated with matching equation in MNs designing as discussed in [37] leads to circuit and layout's more simplicity. In this work, this extra 90° phase is split into IMNs, ISMNs, OMNs, and they are all optimized to present maximum power and 90° desired phase when PA_{aux} is active.

2.4. Input power divider

For the sake of a simple phase difference compensation, the signal path from input to the first stage of each of PA_{main} and PA_{aux} should be equilibrium. Consequently, a symmetric lumped-element Wilkinson power divider with two precisely similar parallel second-harmonic rejection networks on each branch is used. This power divider delivers the maximum power of 11.5 dBm to each of the amplification paths. Fig.4 indicates the performance of this divider.

Fig4. Delivered power to both paths of amplification by Wilkinson power divider.

2.5. Performance comparison with the conventional load modulation based design

This work is designed grounded on a premise, which is made to develop load modulation, now it is mandatory to scrutinize what will be the result of DPA designing if $Z_{out,main}$'s variation is not modeled. To make this comparison, we also designed a DPA without any current compensation, $i_{aux}/i_{main} = 1$. It should be noticed that for the sake of applying the effect of $Z_{out,main}$ variation in the low-power region, in CCLM design, PA_{main} 's matching networks are designed for the worst case of Γ in that region. Fig.5 depicts the change of $Z_{out,main}$ of two designs in which it is evident that CCML case depicts a modified slope in the high-power region in comparison to this case's slope of $Z_{out,main}$ change at the low-level of input power. That slope modification, which leads to PAE increase, cannot be seen in the conventional modulation based design, and it means that in that case, the load modulation is not correctly done. Fig.6 and Fig.7 show both DPA's P_{out} and PAE by which this fact explicitly can be concluded that premise of constant $Z_{out,main}$ in low power level and modeling its change in high power level solely with i_{aux}/i_{main} factor, as it did in conventional DPA, doesn't necessarily lead to reach the best possible performance of PA. It is worthwhile to notice that CCLM cannot be generalized with linear assumptions to all other technologies; according to $Z_{out,main}$ trajectory, designers should take the appropriate strategy for their design. For the sake of linearity assessment, power gain compression of both DPAs is depicted in Fig.8 in which no more than 1 dB gain compression has occurred. Table 1 represents the performances of both designs.

Table 1. Comparison of CCML and Conventional load modulation based DPA performances

	$P_{out} (dBm)$	$P_{out @ 2^{nd} \text{ Harmonic}} (dBm)$	$P_{out @ 3^{rd} \text{ Harmonic}} (dBm)$	$Gain (dB)$	$PAE (\%)$
CCLM DPA	31.61	-51.7	-80.01	18.1	39.6
Conventional DPA	30.12	-51.15	-72.8	15.87	28.3

Fig5. Variation of $Z_{out,main}$ in two circuits of CCML based DPA and Conventional load modulation based DPA.

Fig6. The output power of CCML based DPA and Conventional load modulation based DPA.

Fig7. PAE of CCLM and Conventional load modulation DPAs.

Fig8. 1dB Power gain compression in the proposed DPA.

2.6. Harmonic consideration

Higher-order harmonic rejection is a method to increase the efficiency of PAs. For the sake of making the efficiency of PA raised as much as possible, it is mandatory to take action against the undesired harmonics. The second harmonics of P_{in} can be rejected if an adequately large impedance is in PA input at that harmonic. According to the discussed merit of the circuit's symmetry, two similar parallel harmonic rejection networks are put in both branches of the power divider. Fig.9 shows the impedance of this network, and Fig.10 depicts that there is no considerable amount of higher-order harmonics in the output signal degrading the efficiency. Fig.11 indicates the proposed CCML based DPA's layout, and Table 2 makes a comparison among this work and the other recent GaAs pHEMT technology-based DPAs' performances.

Fig9. The impedance of the Second-harmonic rejection network in frequency sweep.

Fig10. Output power at 2nd and 3rd harmonics of CCML DPA and Conventional load modulation based DPA (with and without harmonic rejection network).

Fig11. The proposed DPA's layout

3. Results

To model $Z_{out,main}$ change under the premise of modified load modulation, even in low-level power, the proposed DPA is designed in a two-stage structure. The main path has two $8 \times 150 \mu m$ transistors. PA_{main} 's first stage is biased in -1 v and 6.4 V for its gate and drain biases, respectively, and those of the second stages are -1 V and 7.4 V. Under the premise of CCLM, the auxiliary path enjoys four $8 \times 150 \mu m$ two by two paralleled transistors.

Table 2- Performance comparison among the proposed DPA and state of the art DPAs in GaAs technology.

	$P_{out}(dBm)$	$Gain(dB)$	$Freq(GHz)$	$PAE(\%)$	Technology
[38]	< 24	<15	37-41**	<30	GaAs pHEMT 0.1 μm
[39]**	<27	≈ 14	28	≈ 37	GaAs pHEMT 0.1 μm
	<27	≈ 12	45	≈ 35	
[40]****	25.1	7	25.8	16.5	GaAs pHEMT 0.15 μm
[41]****	32.78	11.5	24	<35*	GaAs pHEMT 0.15 μm
This Work	31.61	18.1	8	39.6	GaAs pHEMT 0.25 μm

* All are simulation results except those are specialized.

** Based on the simulation results report, although in the paper, it was claimed that DPA was designed for 37-40 GHz, and in its comparison table, only 40 GHz was reported for frequency.

*** This is a dual-band DPA, and for each band, we reported the best amount of simulation results. The exact amount of most of the criteria is not reported. Therefore, for the code of ethics, each of them has a $\approx$ sign.

**** Measured results. Simulation results were not reported.

* It is estimated, just drain efficiency is reported.

The first stage of PA_{aux} has -1.4 V and 6.9 V for its gate and drain bias, while its second stage is biased in -1.2 V and 7.35 V for the bias of this stage's gate and drain, respectively. To make a comparison between a design with CCLM and another with the conventional load modulation, the results of these two DPAs in the same technology are provided in this paper, and it is concluded that for a technology in which $Z_{out,main}$ shows considerable power-based variation, revision of load modulation is needed. In this work, linear modeling of load modulation is viable, but designers should set premises proper for their own $Z_{out,main}$ trajectory. Results show that CCLM based circuit has the maximum PAE of 39.6%, maximum output power of 31.61dBm, at 8 GHz frequency. Those of the conventional load modulation based circuit are 28.3%, 30.12 dBm, at 8 GHz, respectively. Second harmonic rejection networks are put in both circuits, and there is no destructive amount of second harmonic signal in the output power of both designs, less than -50 dBm.

4. Conclusion

DPA concept is based on the load modulation technique in which $Z_{out,main}$ is assumed constant all over the low-level power region. Besides, the same modulation is used for all technologies, while $Z_{out,main}$ variation with power is not akin at all of them and all ranges of sweeping powers. Therefore, in this work, a revision was applied to the equation of load modulation. Under this modification, a DPA was designed, which reached the maximum PAE of 39.6% at the output power of 31.61dBm. For the sake of presenting a comparison by a condition in which CCML was ignored, another DPA also designed in this work. This conventional DPA design proved that in technologies with the appreciable variation of $Z_{out,main}$, load modulation revision, and $Z_{out,main}$ change modeling should be done. Second harmonic rejection networks were put in the input of both paths, and the amount of second harmonic signal in output power was checked; no significant amount of it was there.

5. Appendix

Amount of the elements of the Proposed DPA

$L_1=0.1$ nH $L_2=2$ nH $L_3=0.85$ nH $L_4=1$ nH $L_5=0.53$ nH $L_6=1$ nH $L_7=1.3$ nH $L_8=2$ nH $L_9=0.7$ nH $L_{10}=0.9$ nH $L_{11}=0.6$ nH $L_{12}=1$ nH $L_{13}=1.25$ nH $L_{14}=1.4$ nH $L_{15}=0.1$ nH $L_{16}=2$ nH $L_{17}=2$ nH $L_{18}=1.2$ nH $L_{19}=2$ nH $L_{20}=1.2$ nH $L_{21}=1.7$ nH $L_{22}=2.6$ nH $L_{23}=0.25$ nH $L_{24}=0.9$ nH $L_{25}=2.5$ nH $L_{26}=1.8$ nH $L_{27}=1.3$ nH $L_{28}=0.95$ nH

$C_1=1$ pF $C_2=0.2$ pF $C_3=0.2$ pF $C_4=0.175$ pF $C_5=0.49$ pF $C_6=1$ pF $C_7=0.3$ pF $C_8=0.3$ pF $C_9=0.32$ pF $C_{10}=0.42$ pF $C_{11}=0.26$ pF $C_{12}=0.22$ pF $C_{13}=0.4$ pF $C_{14}=0.75$ pF $C_{15}=1$ pF $C_{16}=0.3$ pF $C_{17}=0.3$ pF $C_{18}=0.28$ pF $C_{19}=0.3$ pF $C_{20}=0.7$ pF $C_{21}=0.4$ pF $C_{22}=0.7$ pF $C_{23}=0.3$ pF $C_{24}=0.3$ pF $C_{25}=1$ pF $C_{26}=0.2$ pF $C_{27}=0.2$ pF $C_{28}=0.44$ pF $C_{29}=0.15$ pF $C_{30}=0.29$ pF $C_{31}=2$ pF $C_{32}=0.3$ pF $C_{33}=0.3$ pF $C_{34}=0.3$ pF $C_{35}=0.3$ pF $C_{36}=0.19$ pF $C_{37}=0.14$ pF $C_{38}=0.3$ pF $C_{39}=0.37$ pF $C_{40}=0.17$ pF $C_{41}=0.45$ pF $C_{42}=2.65$ pF $C_{43}=0.3$ pF $C_{44}=0.3$ pF $C_{45}=0.3$ pF $C_{46}=0.3$ pF $C_{47}=0.28$ pF $C_{48}=0.15$ pF $C_{49}=0.25$ pF

$R_1=100\ \Omega$, $R_2=R_3=R_4=R_5=20\ \Omega$

Amount of the elements of the conventional load modulation based DPA

$L_1=0.1$ nH $L_2=2$ nH $L_3=0.85$ nH $L_4=1.4$ nH $L_5=1.4$ nH $L_6=1$ nH $L_7=1.3$ nH $L_8=2$ nH $L_9=0.7$ nH $L_{10}=1.4$ nH $L_{11}=1.4$ nH $L_{12}=1$ nH $L_{13}=1.25$ nH $L_{14}=1.4$ nH $L_{15}=0.1$ nH $L_{16}=2$ nH $L_{17}=0.7$ nH $L_{18}=1.4$ nH $L_{19}=1.4$ nH $L_{20}=1$ nH $L_{21}=0.8$ nH $L_{22}=1.4$ nH $L_{23}=1.4$ nH $L_{24}=1$ nH

$C_1=1$ pF $C_2=0.2$ pF $C_3=0.2$ pF $C_4=0.175$ pF $C_5=0.49$ pF $C_6=1$ pF $C_7=0.3$ pF $C_8=0.3$ pF $C_9=0.3$ pF $C_{10}=0.3$ pF $C_{11}=0.26$ pF $C_{12}=0.2$ pF $C_{13}=0.4$ pF $C_{14}=0.75$ pF $C_{15}=1$ pF $C_{16}=0.3$ pF $C_{17}=0.3$ pF $C_{18}=0.3$ pF $C_{19}=0.3$ pF $C_{20}=0.7$ pF $C_{21}=0.4$ pF $C_{22}=0.7$ pF $C_{23}=0.3$ pF $C_{24}=0.3$ pF $C_{25}=1$ pF $C_{26}=0.2$ pF $C_{27}=0.2$ pF $C_{28}=0.27$ pF $C_{29}=0.35$ pF $C_{30}=0.4$ pF $C_{31}=0.6$ pF $C_{32}=0.3$ pF $C_{33}=0.3$ pF $C_{34}=0.3$ pF $C_{35}=0.3$ pF $C_{36}=0.3$ pF $C_{37}=0.32$ pF $C_{38}=0.4$ pF $C_{39}=0.17$ pF $C_{40}=0.38$ pF $C_{41}=0.6$ pF $C_{42}=0.2$ pF $C_{43}=0.33$ pF $C_{44}=0.4$ pF $C_{45}=1$ pF $C_{46}=0.3$ pF $C_{47}=0.3$ pF $C_{48}=0.3$ pF $C_{49}=0.3$ pF $C_{50}=0.2$ pF, $C_{51}=0.4$ pF $C_{52}=0.3$ pF, $C_{53}=0.5$ pF

$R_1=100\ \Omega$, $R_2=R_3=R_4=R_5=20\ \Omega$

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